ABSTRACT OF THE DISCLOSURE

Flash memory cells have a split-gate structure in which the channel region underlies a floating gate of minimum lithography dimension, as well as one or more portions of the control gate that extend along one or more sidewalls of the floating gate. The length of the channel underlying the control gate sidewall portions is independent of the thickness of the floating gate sidewall portions and is smaller than and independent of the minimum lithography dimension. Preferably, the control gate is part of a continuous word line extending over a row of many substantially identical memory cells. Channel length need be no longer that the minimum lithography dimension (the channel portion underlying the floating gate) plus a sufficient additional length to account for the thickness of the inter-poly dielectric on the control gate sidewall or sidewalls, and for sufficient direct control of the channel by the control gate.